Analysis and Simulations of Space Radiation Induced Single Event Effects and Transients

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INTRODUCTION

Spacecraft electronic are affected by the space radiation environment. Among the different types of radiation effects that can affect spacecraft electronics is the single event transient (SET). The space environment is responsible for many of the single event transients which can upset the performance of the spacecraft avionics hardware. In this chapter we first explore the origins of single event transients, then explore the modeling of a single event transient in digital and analog circuit. The chapter also addresses the concept of crosstalk that could develop among digital circuits in the present of a SET event. The chapter also provides a discussion of SET hardening**.** We then provide a discussion concerning propagation of a single event transient event at the local, subsystem, and system level in a spacecraft using two different models, one of the models developed by the author, known as the state transition model. The final goal of the chapter is to provide a qualitatively methodology for assessing single event transients and its effects so that spacecraft avionics engineers can develop either hardware or software countermeasures in their designs. SET is not a form of electromagnetic interference (EMI) in its origin, but semantically SET is very similar to EMI because they are both caused a current source not previously accounted for. SET has the same effects as EMI and it can cause interference problems in electronic circuits via multiple coupling mechanisms similar to EMI, and therefore makes such circuits incompatible.

I THE SPACE RADIATION ENVIRONMENT

The dominant energy source of the space radiation environment in the solar system is the Sun. The main effect of the Sun on the space environment is through its electromagnetic flux and the large number of charged particles it emits. The solar particle flux is composed basically of two main components: high energy plasma (E> 1 MeV) bursts (e.g., from solar flares) and the lower energy (E ≈ 10-100 eV) plasma, referred to as the solar wind. The high energy plasma is primarily responsible for Single Event Effects (SEE). Heavy ions or protons striking sensitive junctions in semiconductors and depositing energy causes SEE. These effects range from simple upsets on normal circuit operations to permanent circuit failures. Figure. 1 shows the main sources of energetic particles that cause SEE events: solar energetic particles, cosmic ray protons and heavy ions, and protons and heavy ions from solar flares. Spacecraft electronic are affected by the space radiation environment [1].

[1] The research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

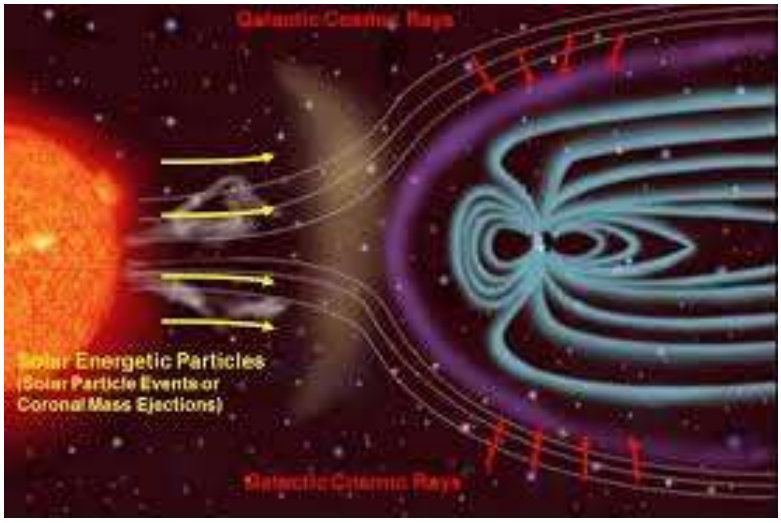

Figure 1. The nature of the space radiation environment

II. SINGLE EVENT EFFECTS

Single Event Effect or SEE is the general term used when space energetic particles are capable of creating an electrical response in an electronics device. All SEE events involves an electrical response observed following the generation of mobile electron-hole pairs by an energetic particle in a semiconductor device. The ionization caused by these energetic charged particles can cause either direct ionization or indirect ionization. Direct ionization, which is the most common, occurs when the incident charged particle creates electron-hole pairs. Indirect ionization occurs when the incident charge particle creates an energetic recoil charge particle, part of the nucleus of a target atom recoils, and then creates electron-hole pairs. Electronic devices that are susceptible to SEE have a level of immunity which is called “threshold LET”. The threshold LET is defined as the minimum Linear Energy Transfer (LET) that can cause a SEE.

The device SEE susceptibility to a specified type of charge particle is usually described in terms of a cross section which is defined as the number of errors observed divided by the fluence required to produce those errors. The single-event upset (SEU), a type of SEE, is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing, the medium through which they pass, leaving behind a wake of electron-hole pairs." SEUs are soft errors of a transient nature in ICs, but are generally non-destructive to the hardware or the IC. Often, a power reset or functional reset of the device is all that it takes for resuming normal operations of the device. SEUs can occur in analog, digital, optical, and mix analog/digital components and they can affect also the interface circuitry (a common cause of failure propagation among circuits). SEUs can appear as transient signals in analog or digital circuitry or as erroneous bits in registers and digital gates. Other possibilities include multiple-bit SEU which are caused when a single ion induces SEUs in multiple bits simultaneously. When there are multiple-bit SEU there is a serious problem in the capability of single-bit error detection and correction (EDAC) of the

system because it is very difficult to assign bits to fill in a word in different ICs; this is especially true in memory ICs. When a SEU is severe it can cause a single-event functional interrupt (SEFI) in which an SEU in the IC, that provides control circuitry, places the circuit into a test mode, halt, or undefined state. A SEFI event interrupts normal operations of the circuitry and requires a power reset for the device to recover its functionality. A SEU in shift registers can also causes a SEFI if these registers control the address of the control logic, resulting in a misread of information in a device. The present trends in electronics development is in the decrease of electronic size scalability and increase functionalities which will increase the susceptibility to SEU and SEFI.

Another type of SEE is the Single-event Latch up (SEL) which causes loss of device functionality due to a single-event induced current state. SELs are hard failures in ICs, and can be highly destructive because it can cause permanent damage in the device. The SEL can cause a high current effect in a given device, which may exceed the device specifications and will damage the device due to local joule heating. A latch up condition can destroy the device, stress the bus voltage, or damage the power supply. A latch up can be caused by heavy ion or by protons impacting very sensitive devices. A SEL can be cleared by a power reset or power strobing of the device. In a latchup condition power must be removed quickly, otherwise a catastrophic failure can occur due to excessive heating or metallization or bond wire failure. SEL is strongly dependent on temperature and the threshold for latchup decreases at high temperature.

A Single-event burnout (SEB) can cause the destruction of a transistor due to a high current surge in a power transistor when a heavy ion passing through the power transistor deposits enough charge to surge that current. SEB causes the device to fail permanently. SEBs can include burnout of power MOSFETs, and frozen bits. Only SEB of n-channel power MOSFETs have been reported. A SEB can be triggered in a power MOSFET biased in the OFF state (i.e., blocking a high drain-source voltage) SEB susceptibility decreases with increasing temperature. SEB can also occur in bipolar junction transistors (BJTs) but are less common.

III SINGLE EVENT TRANSIENT

In this chapter we concentrate a lot in a type of SEE that can cause transients currents propagation, known as the single event transient (SET). SET can not only cause propagation of transient currents within a system but it can also couple to other electronics and systems via parasitic effects.

As electronic components have become smaller in device geometry, lower in operating voltage, and higher in complexity, their immunity to the space radiation environment has been diminished. SET on electronic hardware has become a major concern for spacecraft avionics designers. The spacecraft avionics must be designed such that no single event transient can cause an unrecoverable failure to the spacecraft. When a space charged particle strikes at a sensitive node such as the drain node in an IC, electron-hole pairs are created along an ionization track. A transient current pulse is generated following the drift and diffusion mechanisms. The current pulse results in an single event transient voltage generation at the particle hit node. Under favorable conditions, the pulse will propagate and cause soft errors in additional ICs and their

derived digital cicuits. The measured magnitude, pulse width, and shape of the transient pulse depends on the technology where the SET pulse is generated. Figure 2 illustrates a typical SET pulse and its parameters. Notice that transients can be very large and their pulse with varies considerably.

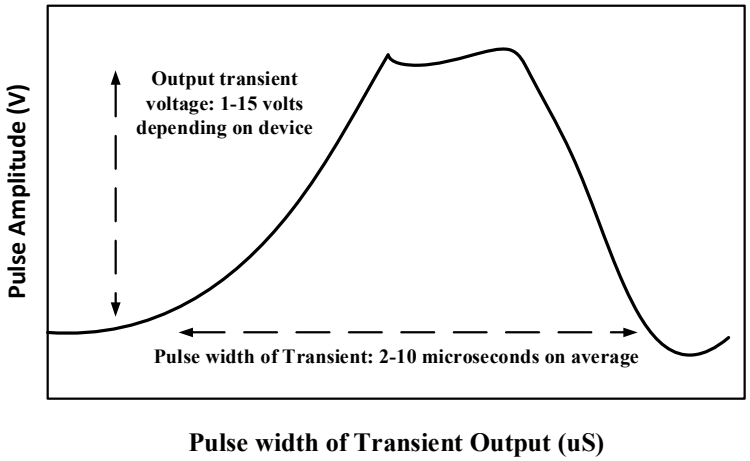

Figure 2. Typical measured parameters in a SET pulse.

When a charge particle travels in space and strikes an electronic IC it interact with the electrons of holes of inside the IC via Electrostatic forces as shown in Figure 3 and discussed in [2-4]. Figure 4 shows the same illustration using a real IC gate. The three main types of interaction are excitation, ionization and bremsstrahlung. In excitations the charge particle transfers some of its energy to the electrons in the IC with insufficient energy to ionize them.

When the electrons decay they emit photons in a process called fluorescence. In ionization, the energy transferred to the electrons is sufficient to cause ionization within the IC material causing the generation of electro-holes pairs. Finally, if the electrons created by the original ionization produces additional ionization, these are called delta rays. Bremsstrahlung, the mechanism by which x-rays are produced, is when photons are emitted, in the form of electromagnetic radiation, when a fast moving charge particle loose some of its energy upon being accelerated and deflected by the electric field surrounding the positively charge atomic nucleus.

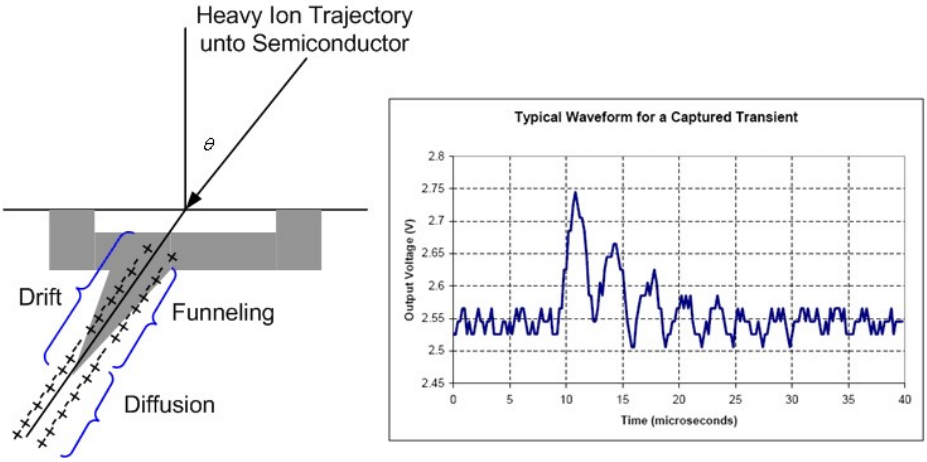

Figure 3. The generation of electron-hole pairs (ionization) and the resulting transient pulse from a single event transient.

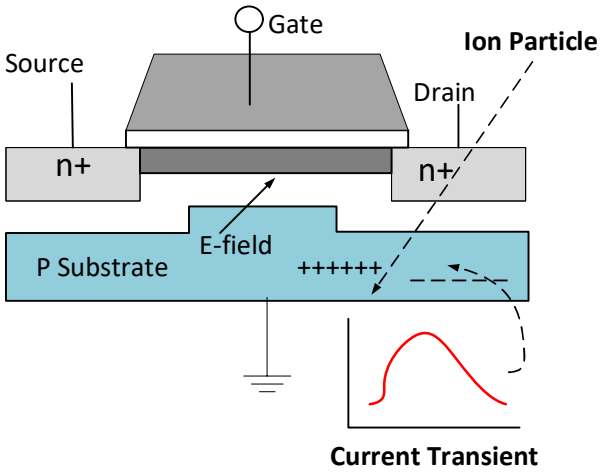

Figure 4. Illustration of the generation of electron-hole pairs in a gate.

IV. GENERATION AND MODELING A SINGLE EVENT TRANSIENT.

Space charge particles such photons, electrons, protons, and heavy ions are capable of ionization when these charge particle penetrate through semiconductor matter. The energy that is loss by an ionizing particle when it propagates through matter is called linear energy transfer (LET). LET is defined as the total energy that is loss per unit distance of travel and it is normalized by dividing the energy per unit distance by the density of the matter in order to obtain units that are KeV-cm^2/mg. The normalization makes LET for a charge particle and energy about the same for different materials. The formula is given by equation 1which is well known in the SET literature.

$$\text{LET}=\frac{4\pi k_e^2 Z^2 e^4 n}{m_e c^2 \beta^2}\left[\log_e\left(\frac{2m_e c^2 \beta^2}{I(1-\beta^2)}\right)-\beta^2\right] \qquad (1)$$

where

A = atomic number of the absorber (absorber in our context of electronics is the semiconductor material), c = speed of light m/s; e = magnitude of the charge of the electron, in C; I = mean excitation energy of the absorber in J; k_e= Coulomb constant Nm^2/C^2; m_e = electron rest mass in Kg; n = N_A ρz/A = number of absorber electrons per unit value, electrons^{-3} or $n=\frac{N_A \rho \eta}{M}$; N_A = Avogadro's number, Kg Kmol; η = number of electrons per molecule of absorber; M = molecular mass of absorber, kg/kmol; v = velocity m/s; Z = atomic number of the incident particle; $\beta = vc^{-1} = \left(\frac{2E_k}{E_0}\right)^{1/2}$; ρ = density of the absorber, kg/m^3; E_k = kinetic energy of the incident particle (eV); $E_0 = mc^2$ = rest energy of the incident particle (eV); and m = rest mass = eV/c^2

The charge deposition for a striking particle with a given LET and with a penetration D is given by equation 2.

$$E_{deposited}(eV) = LET_{\rho} D(cm) \rho \qquad (2)$$

where ρ=density, g/cm^3. The charge deposited is given by equation 3.

$$Q = \frac{E_{deposited} * e}{I_{first}} \qquad (3)$$

where I_{first} = first ionization energy of the atoms in the absorber, eV. It is the energy required to remove one or more electrons from a neutral atom to form a positive ion. For example, for silicon (Si) is 3.62eV, for germanium (Ge) is 2.98eV, and for gallium arsenide (GeAs) is 4.8eV; e = magnitude of electron charge, C; and Q = charge deposited, C.

Of great interest however, is the calculation of the *upset rate* for a given IC as a function of LET. The upset rate is defined as the number of times an impacted IC causes the circuit to have an erroneous output. Therefore, in order to know if an IC is experiencing a SEE, its corresponding circuit output must be detected either at the board level or assembly level. An accurate method for calculating the upset rate (upsets/day) is the usage of the Weibull distribution [5] function F which would have the form

$$F(LET) = \sigma\left\{1 - e^{-\left[\frac{(LET - LET_{threshold})}{w}\right]^s}\right\} \qquad \text{for LET} > \text{LET}_{\text{threshold}}$$

$$F(LET) = 0 \qquad \text{for LET} < \text{LET}_{\text{threshold}} \quad , \qquad (4)$$

where "w" is the width of the distribution and "s" is a shape parameter (s = 1 corresponds to an exponential distribution, s = 2 corresponds to a Rayleigh distribution, s = 4 approximates a normal distribution, while large "s" approaches the log-normal distribution). σ is the value of the limiting cross-section, with typical units of cross-section in cm^2 per bit.

In Table 1 we can observe a numerical application of the formulas previously derived for a series of common ICs in a given circuit application. The application is that of an IO bus, for this particular example, and the environment is that of low earth geosynchronous orbit (1470 km at 53^0 inclination orbit) in a predominant proton environment. The "usage factor" for the ICs in Table 1 is hypothetical for a typical IO bus.

Part Type	σ (cm^2/bit)	LET_{th}	Weibull "s"	Weibull "w"	#Bits /device	Bit SEE (rate /day)	Device SEE (rate /day)	Usage Factor of IC in PCB
FPGA	2.3E-06	24.99	0.741	22.55	140	1.2E-08	1.6E-06	26%
256k SRAM	6.0E-06	29.44	3.923	15.91	262144	1.7E-14	4.5E-09	80%

Op-Amp	1.0E-04	2.89	1.189	35.64	1	3.0E-03	3.0E-03	100%
512k SRAM Asyn	8.8E-09	20	5	100	262144	2.0E-11	5.3E-06	40%
Octal Transparent Latch Tri-state outputs	2.5E-06	40	6.87	28.7	8	1.1E-08	8.4E-08	33%

Table 1. SEE Rate Calculations for an earth 1470 km x 53^0 Inclination Orbit, in a Proton Induced Environment

V. USE OF UPSET RATES FOR ANALYZING VULNERABILITIES OF DESIGNS TO SEE.

For electronic designers it is very important to potentially identify critical components in their design that are susceptible to SEE because such components now become part of a critical path to the failure of the whole design. The concept of critical paths is borrowed from management sciences [6], which states that the success of a project hinges mainly on a few critical paths and these paths are always the most constrained in terms of schedule, funding, and resources. Likewise, from an electronic hardware performance point of view, a critical path is made up of a series of electronic components whose failure are deemed critical because the hardware will fail to reach its design objectives. Failures in critical paths yield critical failures. In most cases critical failures will result in failure to reach mission objectives, and in some cases, actual mission failures.

For each critical hardware assembly, critical circuits are first identified. Once the critical circuits are identified, then critical components are identified. These critical components constitute the critical path(s). This is then followed by assessing which of these critical components are most susceptible to SEE. This assessment is done via analysis. When the assessments are completed, several options can be pursued, ranging from doing nothing about it to recommending design changes.

We now illustrate a simple, but very illustrative example, of analyzing the SEE susceptibility (SET in this case) of several critical paths within a FPGA (only a very small partial design of the FPGA is shown). This approach can also be extended up to the board level. In this example, the FPGA itself has been deemed a critical component for this particular design. However, we intend to extend the SET susceptibility to several critical circuits within the FPGA. For the sake of the example, we will analyze only two of these critical circuits within the FPGA. There may be many critical circuits in the application, and in some cases all the circuits could be critical, though some more than others.

The FPGA under discussion is on a board used to fire several pyrotechnic devices for deployment functions (e.g., a solar array deployment). The FPGA interfaces with the main command and control bus and provides the timing signals and pulse signals for executing the enabling and firing commands on the enabling and firing circuits which are also part of the board.

Two of the circuits within the FPGA that were deemed to be critical are the *pulse generator* circuit and the *execute* circuit. These circuits constitute only 5% of the whole FPGA design. The *pulse generator* circuit (Figure 5) provides the pulse timing, pulse shaping, and pulse duration for the enabling and firing circuits. The *execute* circuit (Figure 6) guides and controls the execution of the pulse generator circuit.

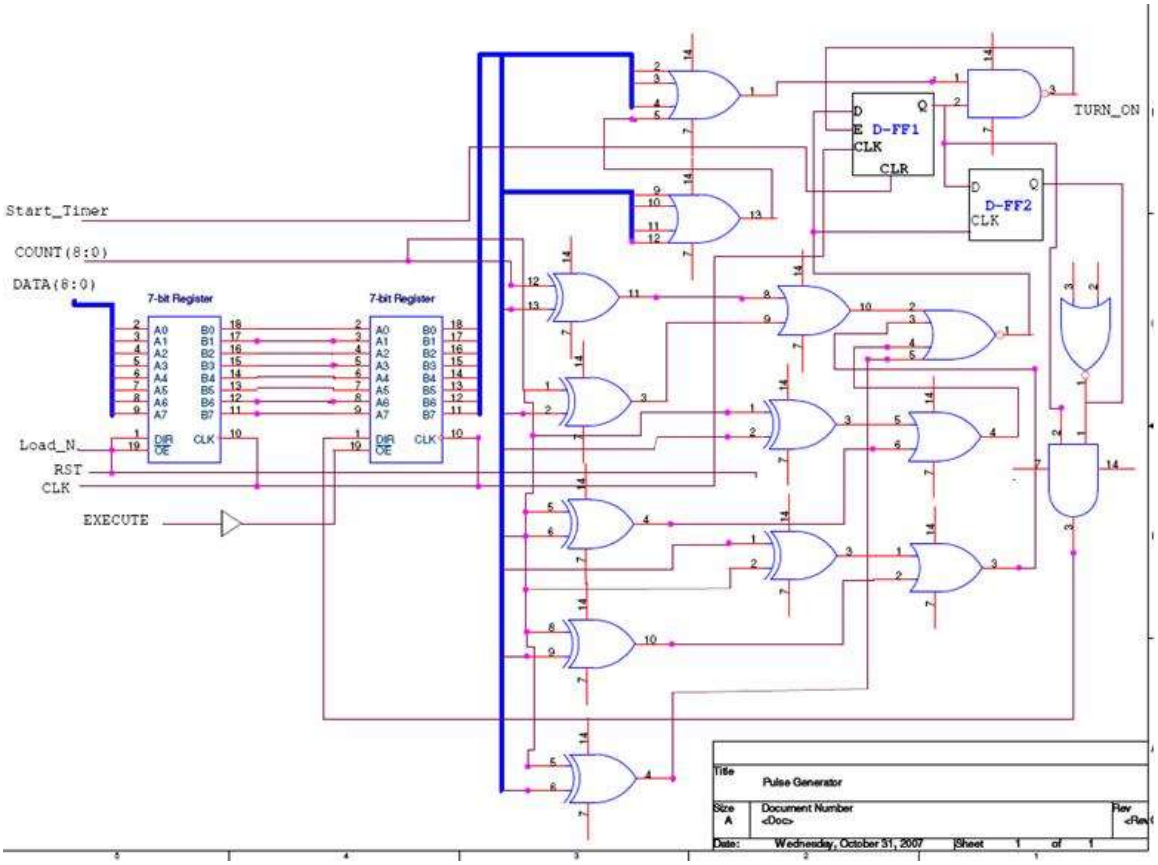

Figure 5. Pulse generator circuit.

One of the serious failures identified that could be caused by an SET event is *to drive an output shorter or longer than intended while firing.* The probabilities for such an event to happen can be measured as the mean time between failures (MTBF).

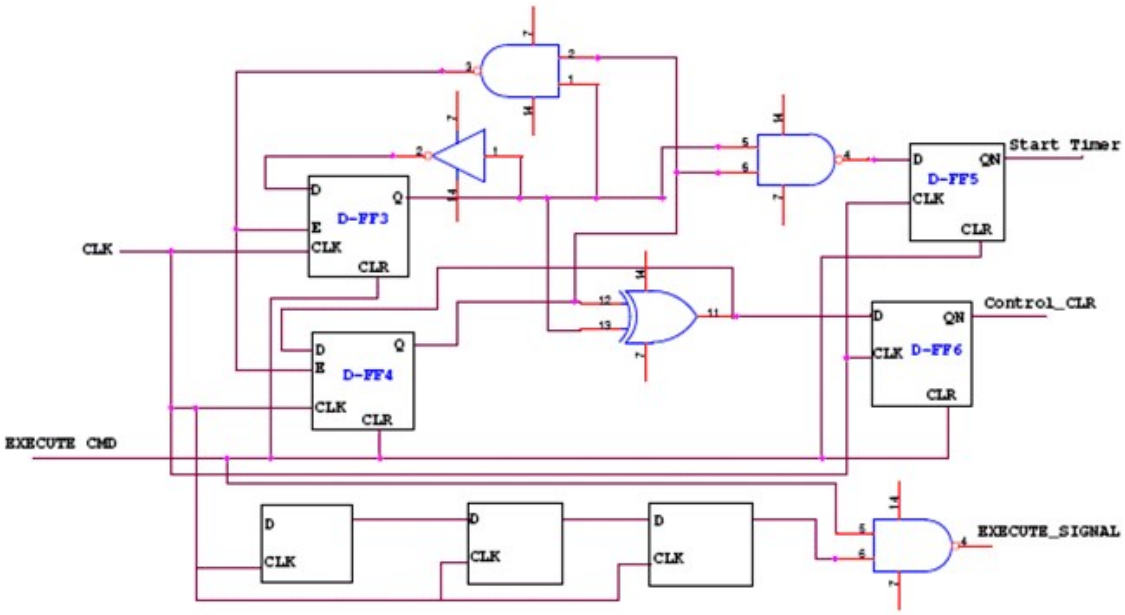

Figure 6. The execute circuit.

There are four SET effects that could cause the above failure to happen:

(1) SET will cause changes in the duration time in either of the seven bit registers in the pulse generator circuit in Figure 11. This would have to occur sometime between the issuance of an enable and a fire command. From Figure 11,

Device (register) "normal" upset rate, per gate, at geosynchronous orbit= 2.1×10^{-5} upsets/day. For two whole registers, the upset rate = 7(outputs) x 2(registers) x 2.1×10^{-5} upsets/day; MTBF = $1/\{7 \times 2 \times 2.1 \times 10^{-5}\}$ = 23809 days/upset.

In a "high" solar flares environment upset rate, per gate, at geosynchronous orbit = 4.9×10^{-2} upsets/day; MTBF = $1/\{7 \times 2 \times 4.9 \times 10^{-2}\}$ = 1.4 days/upset.

(2) The master counter in Figure 11 gets a SET and skips over the duration. This would cause the fire command to last several tenths of msec extra. SET would have to occur in one of the top six least significant bits of the master control.

Devices ("X-OR" and "OR" gates) "normal" upset rate, per gate, at geosynchronous orbit= 7.8×10^{-5} upsets/day. For the total of 6 outputs of the gates, the upset rate = 6(outputs) x 7.8×10^{-5} upsets/day; MTBF = $1/\{6 \times 7.8 \times 10^{-5}\}$ = 2136 days/upset.

In a "high" solar flares environment upset rate, per gate, at geosynchronous orbit = 10.2×10^{-2} upsets/day; MTBF = $1/\{6 \times 10.2 \times 10^{-2}\}$ = 1.63 days/upset.

(3) CNTR_CLR in Figure 12 (Execute block) goes off during fire pulse and resets the master control before the counter reaches duration. D-FF6 would have to flip low to high in the execute block.

Devices (D-FF) "normal" upset rate, per gate, at geosynchronous orbit= 9.6 x 10^{-8} upsets/day. For two flip flops (D-FF5, DFF6), the upset rate = 2(outputs) x 9.6 x 10^{-8} upsets/day; MTBF = 1/ {2x9.6 x 10^{-8}} = 5208333 days/upset.

In a "high" solar flares environment upset rate, per gate, at geosynchronous orbit = 1.2 x 10^{-4} upsets/day; MTBF = 1/{2x1.2 x 10^{-4}} = 4166 days/upset.

(4) D-FF4 in Figure 12 gets an SET (low to high) during a fire pulse.

Devices (D-FF) "normal" upset rate, per gate, at geosynchronous orbit= 9.6 x 10^{-8} upsets/day. For two whole registers, the upset rate = 2 x 6(outputs) x 9.6 x 10^{-8} upsets/day
MTBF = 1/ 2 x 6{9.6 x 10^{-8}} = 868055 days/upset

In a "high" solar flares environment upset rate, per gate, at geosynchronous orbit = 1.2 x 10^{-4} upsets/day
MTBF = 1/ 2 x6 {1.2 x 10^{-4}} = 694 days/upsets

After this analysis we can proceed with assessing which components have the lowest MTBF as being the most susceptible. In the example described, it is the counter, especially in a high flare environment with the higher probability of getting an upset. We compare the MTBF of the most susceptible components with the mission function and assess the probabilities of having SET upsets during the particular mission function for those particular components. It is obvious from the example, that no pyrotechnic functions should be attempted in the spacecraft during a solar flare event. As a following step, if a given mission function can't be avoided, it is then important to assess the circuit behavior consequences of those upsets and this assessment will result in further action, ranging from "we can live with it" to hardware redesigns.

Other options for improving space radiation immunity is boosting the common mode operating rage of a part, current limiting the power supply bias and providing localized shielding.

VI. CIRCUIT MODELING OF SINGLE EVENT TRANSIENTS.

For modeling purposes (e.g. SPICE simulator) the current pulse generated is usually modeled using a double exponential waveform [7] as shown in equation 5. Q is the charge (positive or negative) deposited by the particle strike and given by equation 3, τ_α is the collection time constant of the p-n junction, and τ_β is the ion-track establishment time constant. The time constants τ_α and τ_β are dependent on process technology and can be taken as 0.1 nS and 0.05 nS, respectively.

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha} - \frac{t}{\tau_\beta}}\right) \qquad (5)$$

A charge injection circuit for SPICE simulation is represented in Figure 7 as an independent current source where I(t) is given by equation 5.

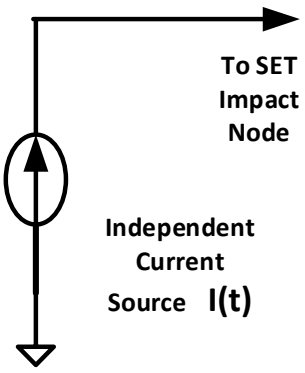

Figure 7. Charge Injection Circuit Model

An example on the use of such a current injection model is the circuit shown in Figure 8. In the figure, the induced transient current source is simulated at the output of a digiatal gate and propagating to another gate where it will cause the wrong output on such gate.

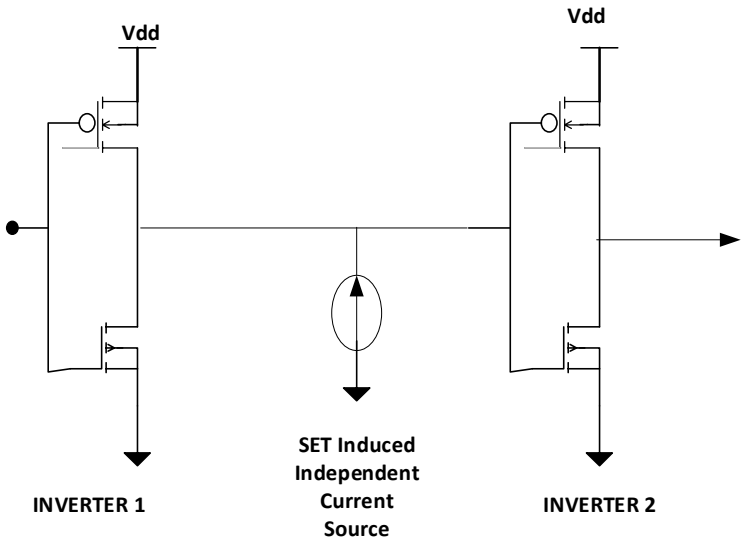

Figure 8. Modeling a SET induced current transient inside an digital gate.

The main problem in modeling an independent current source as shown in Figure 8 relates to the accuracy of the transient current used as the input stimulus. The model of the transient current source can affect considerably the circuit simulation accuracy. A typical example is the resulting SET current resulting from the device-level simulation of an unloaded device. In these cases the circuit simulation inherits the inaccuracy of the improperly loaded device simulation.

The previous outlined limitations of circuit level simulation can be overcome by using physically-based device simulation to predict the response to ionizing radiation of the affected device. This approach is referred to as “mixed-mode” or “mixed-level” simulation, since the struck device is described by simulation in the device domain and the other devices by circuit models. The two simulation domains are tied together by the boundary conditions at the circuits, and the solution to both sets of equations is rolled into a single matrix solution. However, the

main inconvenient of the mixed-level simulation approach is the increased CPU time compared with a full circuit-level (SPICE) approach. In addition, mixed-mode simulation becomes not tractable for complex circuits. Therefore, in this chapter we advocate for the circuit level simulation model as descibed in Figure 8 as sufficient for analyzing SET events.

Because we are often only interested in the behavior of an overall circuit to a SET event, a different approach should be followed. Rather than modeling the internals of the linear IC in order to assess the SET effects on the outputs of the IC, an easier approach is to model just the SET transient on the IC output only. We can then propagate the behavior of the SET to the overall circuit. This approach is illustrated in Figure 9 where a transient pulse is modeled via SPICE on the output of U2. The transient is modeled as V3 using a pulse step function in SPICE. The magnitude of the voltage step function can be modeled from equation 5 and the use of a dummy resistive load in the V3 voltage source. We can then capture the pulse response effect at the circuit load (represented by C2 || R5). It is important to realize using the example of Figure 9 that a SET is capable of causing serious detrimental effects in a circuit's performance. In the example of Figure 9, it is shown that a SET transient can inadvertently turn-on the MOSFET and momenterely activate the circuit even if it was not suppose to. The inadvertent activation of the circuit can result in detrimental effects dowstream from where the circuit is located.

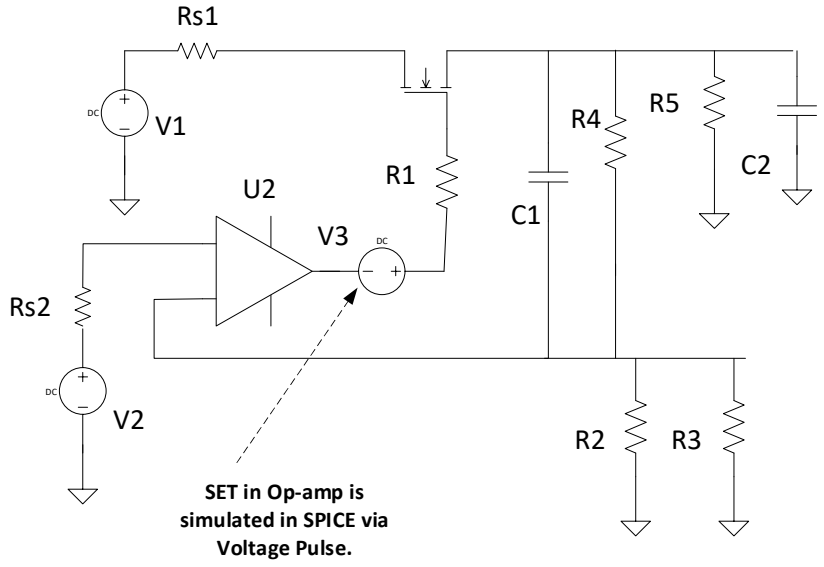

Figure 9. Modeling a pulse (V3) at the output of a SET suceptible device (U2)

VII. SINGLE EVENT TRANSIENTS IN DIGITAL DEVICES

Advanced digital microelectronic technologies are often more susceptible to single-event effects more than other previous technologies developed over the past thirty years. Because of the factor related to technology scaling there is now a greater sensitivity to single-event upset in memory integrated circuits than ever before. Digital single-event transients in high-speed electronic ICs have also become a growing concern and specially in space systems. Digital SET (DSET) are transient voltages or currents occur in a digital circuit that has been struck by a high energy particle, even though the strike may not cause an upset in the circuit struck by an energetic

particle [8]. The transient effect can propagate through subsequent circuitry and will eventually cause an SEU when the transient event reaches a latch or other memory element. There are mainly four criteria that must be met for a DSET to result in a circuit error: 1) the energetic charge particle strike must be able to generate a transient pulse capable of propagating through the circuit, 2) there must be an credible logic path through which the transient pulse can propagate to reach at a latch circuit or other memory element circuit, 3) the transient pulse must be of sufficient amplitude and duration to change the state of the latch circuit or memory element circuit, and 4) in synchronous logic electronics, the transient pulse must arrive at the latch circuit during a clock pulse in order to enable the latch. The probability is large that momentary glitches will be captured as valid data in combinational logic, and this probability increases greatly with frequency as the frequency of clock cycles increases. As logic circuits speeds increase, it is also reassured that the ability of a given transient to propagate increases. Due to both, the greater capability of pulses to propagate in high-speed circuits and their higher probability of be captured by subsequent storage elements circuits such as in latches, digital transient pulses have become very common in deep submicron digital electronic circuits. Transients in digital circuits were first observed in the arithmetic logic unit of microprocessor [9]. Digital transient pulses due to strikes in clock logic circuits were reported in the early 1990's [10]. Research data has confirmed the existence of digital single event effect transients in several technologies, such as high-speed GaAs FET [11], Si bipolar [12], and Si CMOS logic circuitry [13], [14]. Several experiments results obtained during the measurements of the properties of digital single event transients in specialized test fixtures have been done in an effort to understand the mechanisms of transient effects which can help in the development of mitigation techniques [15], [16] – [19]. Circuit analyses and modeling techniques have been applied for the purpose of estimating the logic error rates caused by digital single event transients [20], [21] – [23], but few device-level simulations have been performed to research the physical mechanisms involved in DSETs.

Typical sequential elements in the core logic of electronic circuits are the latch, a domino cell or a register file cell. State changes can occur in the core logic of digital circuits similarly to memory elements. In sequential logic (like in SRAM) the soft error rate has been found to be independent of the clock frequency of the circuit [24]. For example, the latch state of a gate can be flipped by the charge deposited by a particle strike on a gate node regardless of the state of the clock signal, as shown in Figure 10.

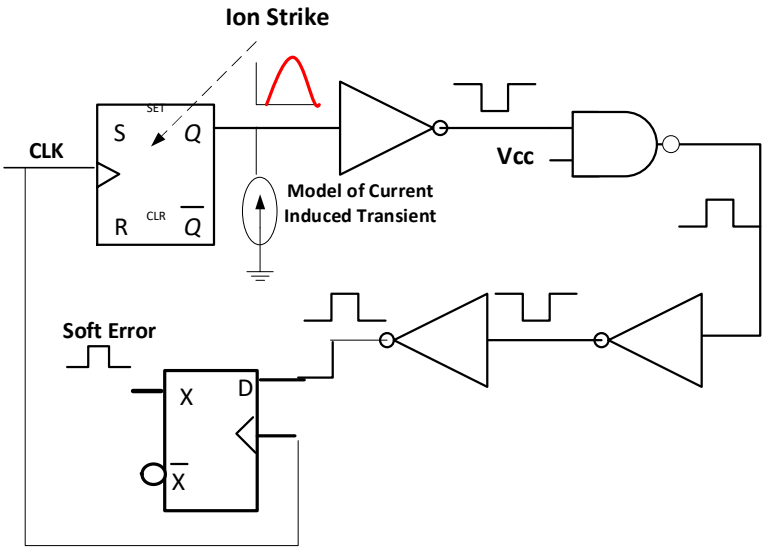

Figure 10. Illustration of SET effect in a synchronous circuit.

Flip-flop circuits and sequential logic circuits are main types of logic circuits. Technology has been scaling down, considerably going to smaller features, and therefore flip-flops have become more susceptible to many types of soft errors. The decrease in supply voltage for flip flops and in their node capacitances has made flip flops more susceptible to single event effects. Flip-flops circuits are similar in design to memory cells, since they both have feedback loops of cross-coupled inverter-pairs. The soft error sensitivity of flip flops and memory circuits is determined by the critical charge that can accumulate in those devices and the collection efficiency. For example, in a SRAM cell the charge accumulation is mainly the same for the two storage nodes because the memory cell is symmetrical. In the case of flip-flops, the inverters are normally sized differently and also they have different fan-outs, which makes the flip-flop circuit asymmetric compared to the SRAM. The individual storage nodes in flip-flops circuits also have a different critical charge per flip flop when compared with SRAM cells and their SET sensitivity can vary by several orders of magnitude.

Any node which is part of a combinational circuit can be susceptible by an SET event and the node is capable of generating a voltage transient which can then propagate through several nodes of the combinational circuits as shown in Figures 11 and 12.

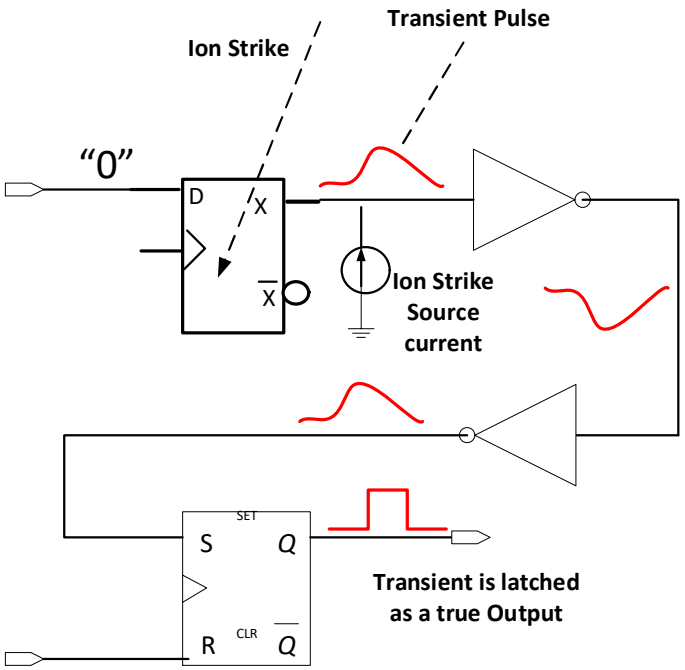

Figure 11. Transient propagation in a FF where transient causes a non-intended output

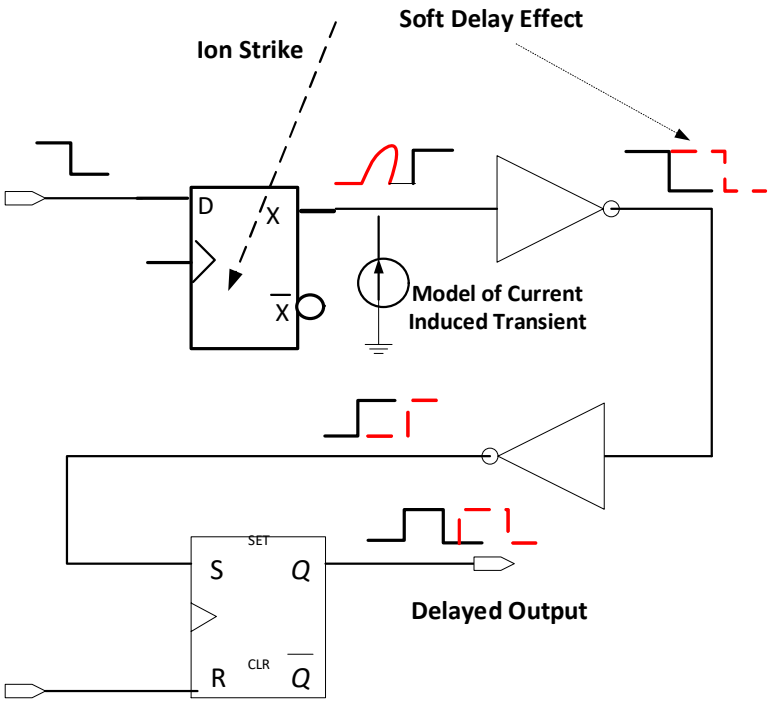

Figure 12. Transient propagation in a FF where transient causes a non-intended delay in the output.

A SET event can cause errors in the gates if the SET event gets latched by a sequential element, such as in a memory cell. In combinational logic components some transient events will be latched and others will not be latched depending on the circuit topology. However, even for the cases where such transient events are latched, some of the data will not be transmitted as errors during software operation. The rationale for this lack of software errors is that a transient event in a logic circuit may not be captured because it could be hidden by one of the following three phenomena: (i) logical hidden response which occurs when a charge particle strikes part of the combinational circuits but it is not capable of affecting the output because subsequent gates outputs are completely determined by other input values from those gates, (ii) latching-window hidden response which occurs when the pulse resulting from a charge particle strike reaches a latch but not at the clock transition time at which the latch can captures its input value. Therefore, the error bit cannot be latched, and there will be no a soft error which would have been the natural consequence, and (iii) electrical hidden response occurs in pulse transients where the bandwidths is larger than the cutoff frequency of the circuit.

VIII. SET-INDUCED CLOCK JITTER AND FALSE CLOCK PULSE

A clock jitter can be induced by a single event transient and occurs when charge particles deposit their charge into the nodes of a clock circuit when the clock edge is present. Therefore, the clock edge can vary and incorrect data may be stored. Figure 13 shows an example of a clock jitter in a flip-flop (FF) configuration where the signals IN, OUT, and CLK denote input, output, and clock signals respectively of the flip-flop. Figure 13 shows the clock of the FF when there is no clock upset due to the lack of a single event-induced charged particle transient. The same figure also shows the clock behavior when there is either a false clock pulse (or jitter) which is induced by a transient event. This jitter will cause the output signal OUT to be delayed as shown in the figure. In the case of the clock jitter, if the output signal "OUT" is connected to another storage element, incorrect data storage can occur when the delayed output signal arrives during the set-up time of the receiving sequential input signal. As shown in the figure, in addition to clock jitter, an energetic particle strike can also create a "false clock" pulse on clock circuit nodes where there is no clock pulse present. If the pulse generated by the strike is of sufficient magnitude and width, it can be mistaken for a real clock signal and can cause unwanted latched behavior in combinatorial circuits.

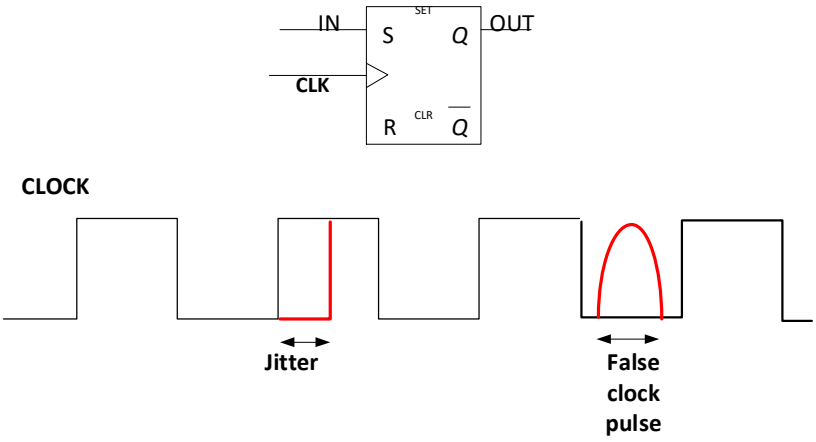

Figure 13. SET induced Jitter and a false clock pulse present in a clock signal.

IX. DESIGNING DIGITAL CIRCUITS FOR *SET* SURVIVABILITY

Two of the most common type of digital circuits are field programmable gate arrays (FPGA) and applications specific interface circuits (ASIC). These ICs are used in large scale digital designs and they are often configured to perform complex communications, control, signal processing, and command functions in spacecraft. In FPGA and ASIC, a straight forward approach to get around SET is to use triple majority redundancy for all critical FPGA registers. Triple majority voting refers to a FPGA register implementation technique in which each FPGA register is implemented by three flip-flops or latches whose votes (two of three) determine the state of the register. Any failed flip flop is out voted by the other two. Triple majority voting can also be applied to complete designs or parts of circuits, no just registers.

The inclusion of triple majority voting can be done directly with very-high-speed-integrated hardware description language (VHDL) source code, which does not require too great of an effort. There are also synthesis tools that can replace any flip flop with a triple majority voting set of three flip flops, without the need for rewriting the VHDL source code.

Some FPGA technologies, such as the SX-S family from Actel (now Microsemi) include triple majority voting flip flops on silicon [25]. This technique should be applied to all crucial designs (including data paths, status and configuration registers), specifically in those applications for which no power cycling or reset is possible. An example of triple majority implementation using a FPGA shift register in an Actel FPGA is shown in Figure. 14. Notice that if one flip flop is accidentally flipped to the wrong state, the other two out-vote it and the correct pulse is propagated to the rest of the circuit. The three “D” flip flops must receive the same inputs and the outputs are compared to select the “two of three” and the result is then passed to the output holding register in the diagram.

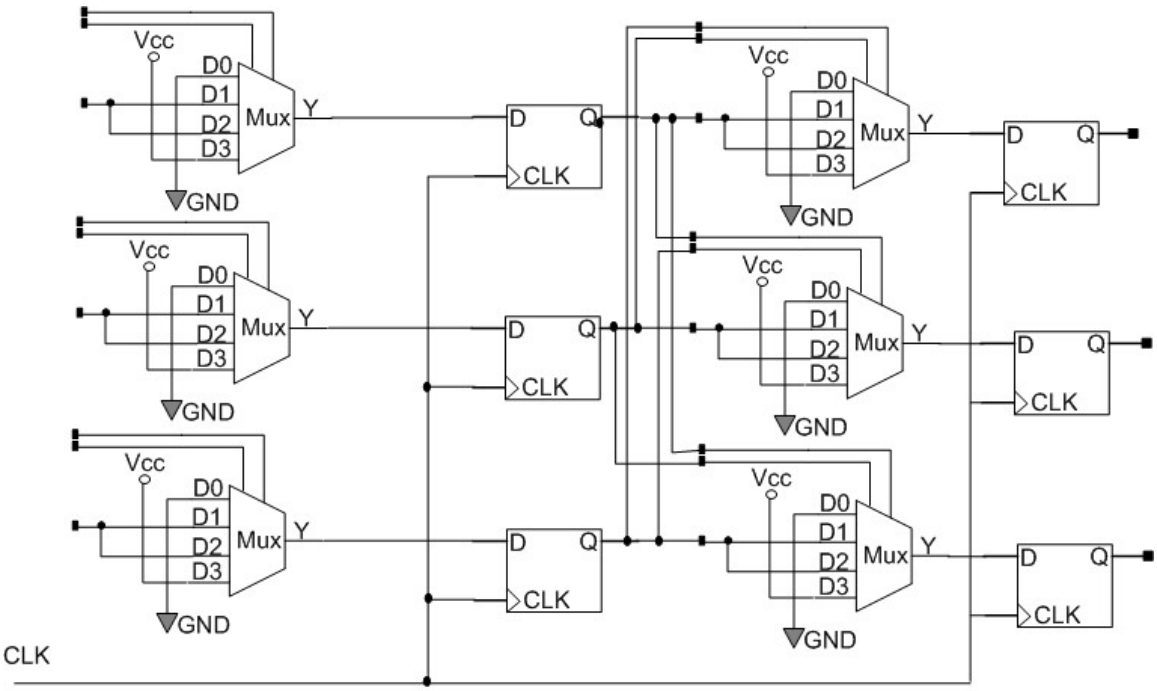

Figure 14. Triple majority voting using separate voters. MUX and flip-flop combine into a single S module. Actel FPGA implementation (with permission from Actel).

Figure 15 shows the basic R-cell functionality of an Actel RT54SX-S FPGA. Figure 16 illustrates a simplified representation of how the D flip-flop in the R-cell is implemented in the SX architecture. The flip-flop consists of a master and a slave latch gated by opposite edges of the clock. Each latch is constructed by feeding back the output of the input stage. The potential problem in a space environment is that either of the latches can change state when hit by an ion with enough LET energy. To achieve SET hardness, the D flip-flop is enhanced (Figure 16). Both the master and slave latches are actually implemented with three latches. The feedback path of each of the three latches is voted with the outputs of the other two latches, hence the name triple majority voting. If one of the three latches is struck by an ion charge and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching. The layout must be such that a single ion can only strike one latch. This approach can be extended to higher level designs within an FPGA, for example Figure 17 shows a conceptual design on the implementation of a triple majority voting in the design of a FPGA shift register. The output "Y" is the result of the majority voting of three samples of the "Direct Input" of the circuit. While majority voting is by far the best approach for eliminating SET in FPGA logic, care must be taken to minimize effects on the majority voter output block.

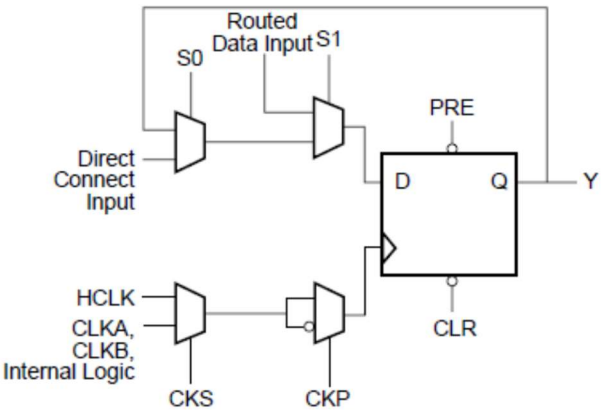

Figure 15. R-Cell functional diagram in a RT54SX-S FPGA (with permission from Actel)

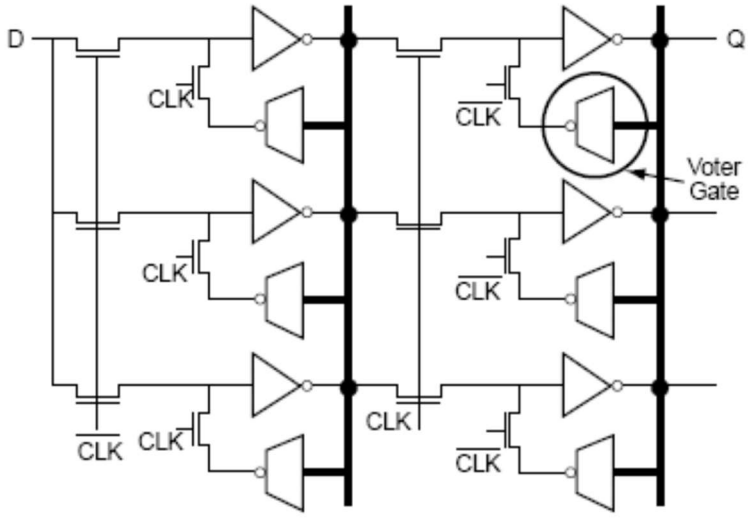

Figure 16. RT54SX-S R-Cell implementation of D flip-flop using voter gate logic.
(with permission from Actel)

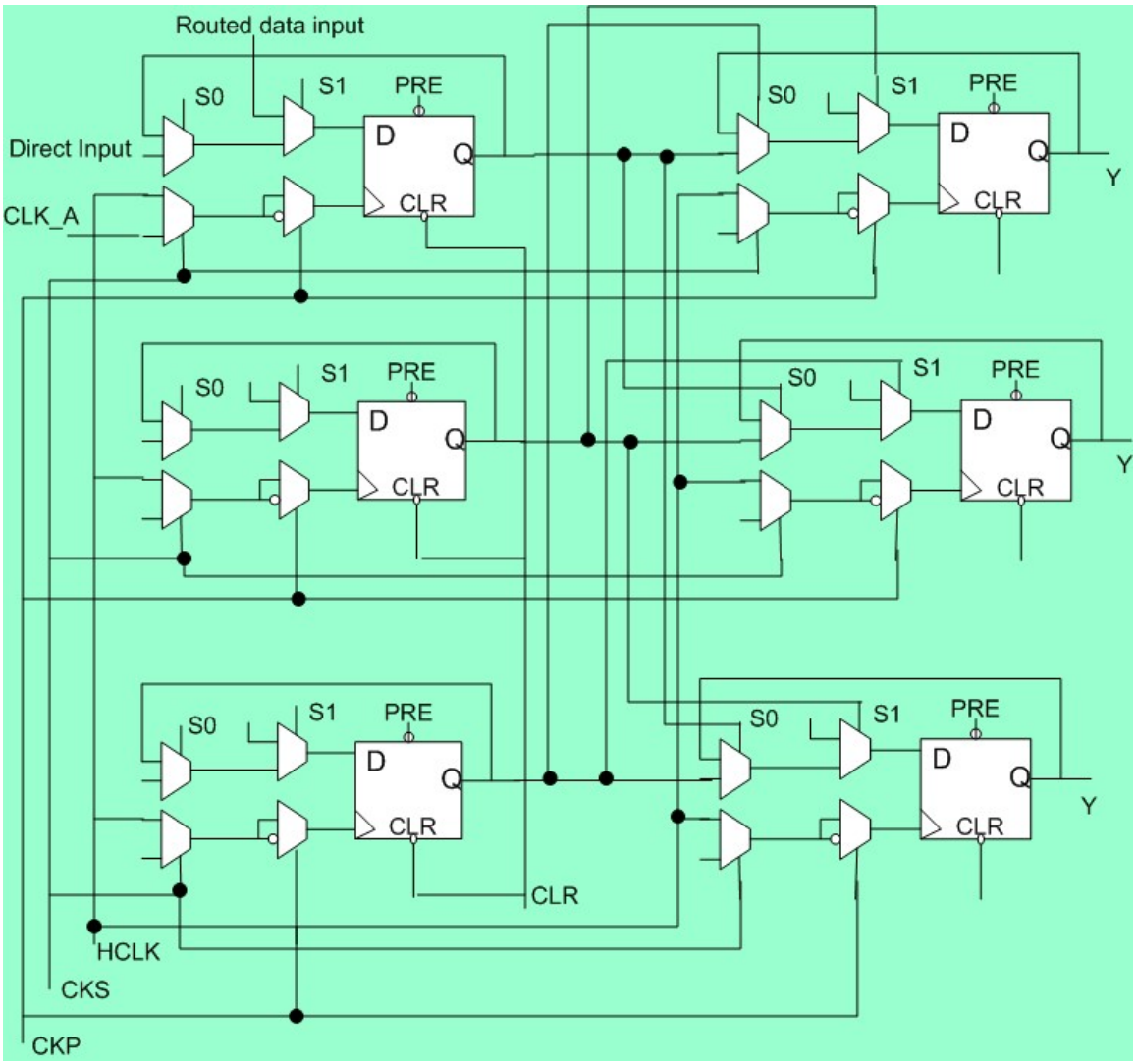

Figure 17. RT54SX triple majority implementation of a FPGA shift register (with permission from Actel).

X. CROSSTALK NOISE FROM SET EVENTS AND DELAY EFFECTS

Design techniques for hardening against single event upsets can produce electronic designs that can reduce, and in some cases eliminate, single event transients in CMOS circuits. Due to the scaling issues in the electronics, coupling effects can increase if spacing between interconnect is reduced and if there is increased thickness to width ratio of interconnects.

The electrical noise interactione caused by parasitic coupling between interconnects of circuits, known as crosstalk, can produce detrimental effects in electronic circuits, such as positive and negative glitches, overshoot, undershoot, and delay changes. If the crosstalk on the victim circuits are large, the crosstalk can propagate to storage memory elements that connect to a victim IC line and can cause permanent errors. Most often normal signal switching on culprit lines are responsible for such crosstalk events. However, as the scaling of technology has continued to decrease, the charge deposited due to an SET hit particle on a culprit IC circuit is

creating increasing coupling noise effects, as can be shown in Figure 18. It can be shown that single event transients by an aggressor IC circuit can create larger noise effects than those transents induced by normal signal switching crosstalk as shown in Figure 19.

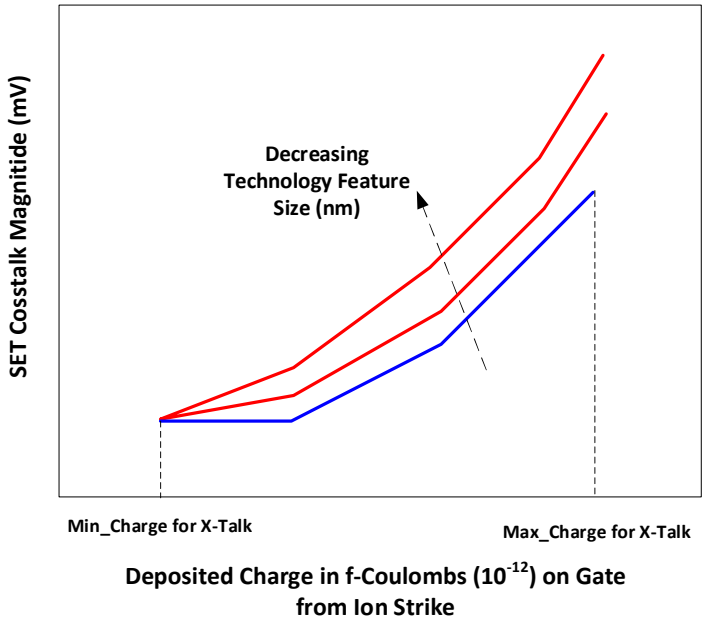

Figure 18. Direct relationship between inclreased crosstalk induced by SET and decrease in IC teachnology feature size.

During the IC layout optimization process used by EDA tools, even though a given net may pass the normal crosstalk noise check, the net may still pose a susceptible scenario if single event transients are not properly considered during the design process. Present EDA tools lack this capability. It is much easier to address single event transients effects during the design process than afterwards when issues are found and modifying the design would cause serious schedule and cost problems.

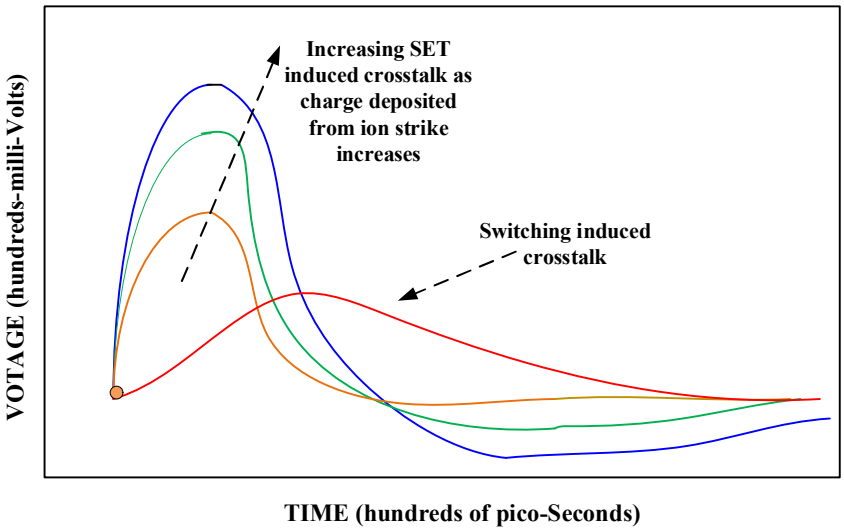

Figure 19. Comparison of Crosstalk induced from SET and from normal switching.

For the circuits which are susceptible to experience coupling effects among its interconnects, as found in the design process, a single event transient pulse which has been generated on a circuit node can affect multiple logic paths in the circuit due to the strong coupling among wires, vias, and even board traces. Figure 20 shows the agressor and the susceptible circuit pair along with its drivers and receivers. In this scenario, when the inputs of both drivers are held at logic 1, the outputs are normally held at logic 0. A SET ion strike at the drain of OFF transistor in the inverter driver can cause the output to go to logic 1 for some pulse duration. The transient voltage created in the culprit circuit can then affect the susceptible circuit through parasitic coupling capacitance, and this will induce a SET crosstalk noise on the susceptible circuit. The coupling effects produced by SET strikes in a circuit can violate the noise margins of gates connected to other affected parts in the circuit and this will result in logic errors as shown in Figure 20a. Large detrimental effects may occur if the susceptible cicuits are of such importance such as in clock cicuits.

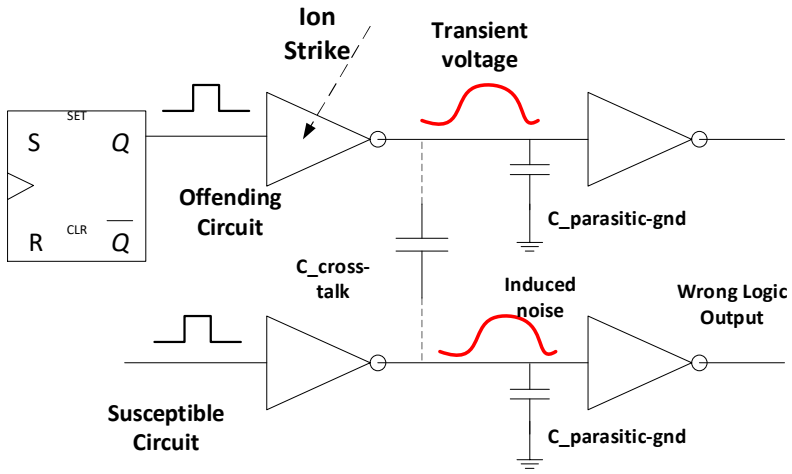

Figure 20a. SET induced crosstalk capable of causing wrong logic outputs.

The SETs generated at the culprit circuits may also cause increased signal delays on a neighboring susceptible circuit such as in switching circuits. This effect can be named SET-induced crosstalk delay. In the example shown in Figure 20b, a SEU particle strikes the output node of the culprit driver and causes a voltage transient to be generated in the culprit circuit. The transient then couples into the suceptible circuit during switching, through capacitance coupling, and causing a signal slowdown on the suceptible circuit. The increase in interconnect delay due to the SET coupling can effect circuit performance. The delay changes cuase by this noise coupling can violate the setup or hold time requirements of logic storage circuits which are connected to these receivers.

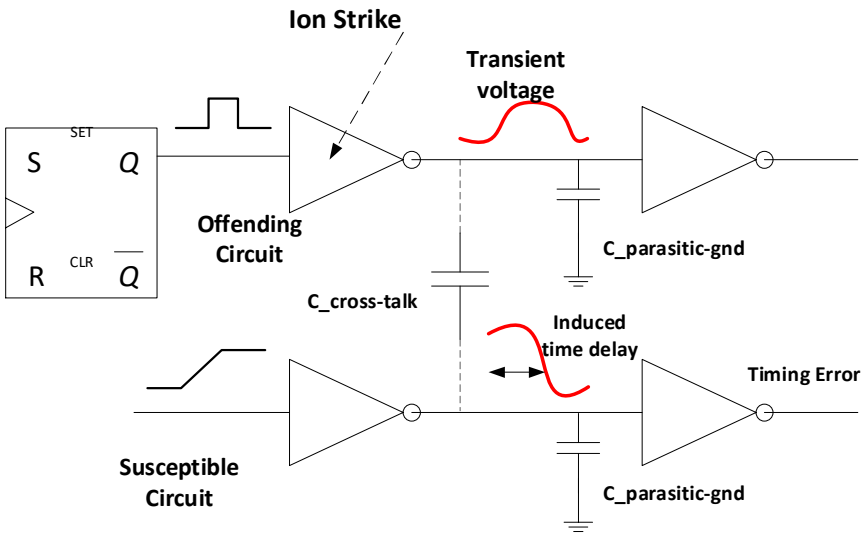

Figure 20b. SET induced crosstalk capable of causing wrong timing delays.

Due the SET induced coupling effects, a single event transient pulse generated on a circuit node can propagate beyond to the propagation path that exists between the affected node and a latch that may reside in the circuit. Therefore, the coupling effects among interconnects in multiple circuits can cause single event upset transients to propagate within electronically unrelated circuit paths, and this can increase the single event transient susceptibility of circuits to single event transients, as shown in Figure 21.

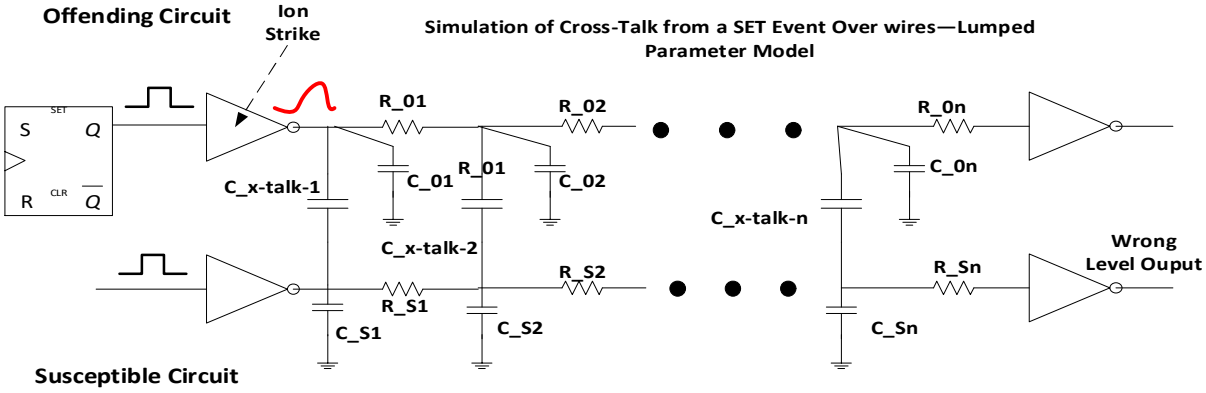

Figure 21. Simulation of crosstalk and SET propagation through adjacent circuits.

Single event transients can induce crosstalk effects on a neighboring electronic component copper paths and can induce logic noise level as small as 100 μV on technologies 90 nm and lower. As the technology scaling goes down there can be an increase in crosstalk effects due to decreased spacing and increased thickness to width ratio of the copper interconnects among

circuits. With enough coupling, a single event pulse can easily spread from one part of the circuit to unrelated parts of combinatorial logic circuit causing single event crosstalk noise effects.

XI SET IN VOLTAGE REGULATORS

The effects of transients in linear devices depend greatly on the circuit application conditions, and this situation makes it difficult to draw conclusion from tests on a specific circuit configuration to other applications with different configurations [26] – [35]. Linear devices in this configuration are the regulators. Regulators are used over a very wide range of input voltages, with input/output voltage differences up to 40 V. The wide range of supply voltages and variation in output loading conditions that we find in regulators are critical parameters that need to be addressed in determining SETs effects in regulators. This flexibility however, increases the complexity of radiation testing, the analysis of SET, and the evaluation of data for regulators concerning during a SET. In studying SETs, the first step is to define the parameters for the amplitude and duration of output voltage response. For voltage regulators, SET with small amplitude or short duration are treated with no much concern, but in reality, these transients can induce unacceptable noise levels in critical circuits. SET with large amplitude can produce voltage conditions that can cause damage to other circuits, or produce noise effects that disrupt normal circuit functions. It must be remembered that the SETs from these regulators are actually occurring even when there is a presence of large capacitor at the device output. This is because the low output impedance and high current capability of these regulator can easily overcome the expected filtering effect of bypass capacitors inside the regulators, and therefore can allow transients to propagate in a network that at first thought may have been immune from such SET effects when a first-order analysis was done by circuit designers

Because voltage regulators are capable of working under a wide range of load conditions it is often difficult to deal with single event transients in voltage regulators, which are intended for use in a wide range of applications. The SET effect on regulators depends on several factors, such as input/output voltage, load capacitance, load current, and operating temperature. All these variables are interdependent of each other and this creates a complex problem for the solution of SET events in voltage regulators.

Just as it is with normal operation in regulators, the transient output voltage from a SET event inside the regulator also depends on the difference between input and output voltage. Therefore, charge generation and collection inside the regulator from a SET strike also depend on voltage conditions, increasing with voltage. These effects are often difficult to model with circuit analysis programs such as those in EDA tools because the modeling accuracy is limited, and it does not incorporate the voltage dependence of charge collection in the internal transistor structures.

SET induced transients from voltage regulators can affect the other circuits fed by the regulator in a variety of ways, increasing the difficulty for engineers of characterizing and defining transient events. Although usually the concern is with transients of high amplitude, voltage regulators can also be use in the regulation of voltage for other circuit cards where small transients can interfere with the normal operation in those cards, and can induce noise that is

greater than the expected interfering with the operations of those cards. Since the threshold LET for low-amplitude transients is very low, it is very likely that protons can induce low amplitude transients in addition to heavy ions.

As discussed in [36] and [37], the circuit designs used in these regulators are complex, using sophisticated design techniques that rely on close matching of various internal transistors. However, there are common ways to reduce the susceptibility of regulators to SETs which do not require a deep understanding of the detailed circuit design. These measures are post design corrective measures and address the circuits outside the regulators. For example, it is quite possible to limit the maximum transient amplitude by adding a circuit that will clamp the voltage between the output of the amplifier and the input to the Darlington output stage, reducing the output voltage transient to mV. The duration of the transients can also be reduced.

Figure 22 shows an example application of an adjustable voltage regulator (LM137) capable of supplying up to 1.5A with an adjustable output voltage Vo that can range from 1.25V to 37V. The output voltage is given by

$$Vo=Vref\,(\,1+ R_2/R_1) +(I_{ADJ} * R_2) \quad (6)$$

I_{adj} is usually around 50uA in most applications and it is often ignored. Vref is defined in Figure 22. The LM 137 regulator (with 26 BJT transistors inside) is susceptible to SET, and a SET will cause V_{ref} to go to zero volts, hence, from equation 1, $I_{ADJ}*R_2=0$. A SET can last from a few microseconds up to tens of microseconds, hence, Vo=0 should last also for the duration of the transient. However, in the circuit of Figure 22, capacitor Co will improve the transient response and C_{ADJ} will greatly improve ripple rejection as it prevents amplification of the ripple as the output voltage is adjusted higher. In this example SET propagation across the circuit has been shown to have little effect, but that is not always the case.

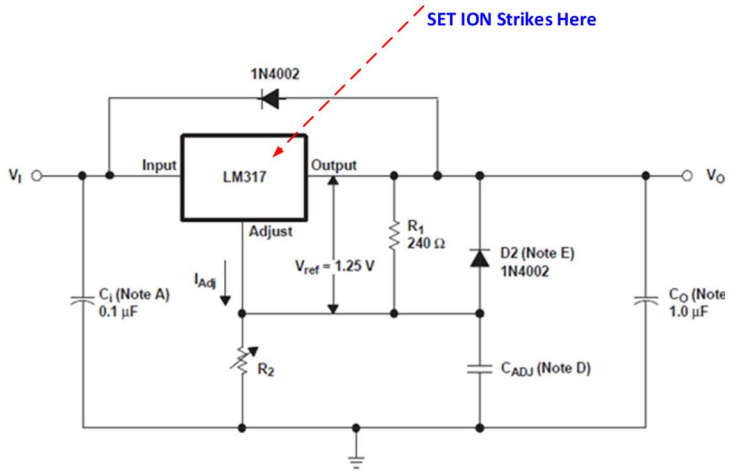

Figure 22. An adjustable voltage regulator susceptible to SET.

XII. SET PROPAGATION THROUGH MULTIPLE CIRCUITS

Transient "glitches" can now be rigorously modeled at the IC level and address its effects within the IC. EDA tools are not capable of doing this modeling but charge transport model tool are capable of providing preliminary data for use in EDA tools.This approach is illustrated in Figure 23 where an ion strike causes a glitch in a transistor gate. The glitch causes the logic to go from logic 0 to logic 1 at the output of the gate. Figure 23 illustrates how such as glitch will ripple through downstream logic causing even more errors on multiple circuits of ever increasing complexity. Even, in clock circuits, as previously shown, a SET can cause momentary glitches which are often recoverable in the next clock cycle but such errors can temporarily interrupt critical function in a space vehicle which can trigger internal alarms and cause emergency "safing" procedures to be executed. For example, work by this author has shown (non-publishable) that a few such events in critical circuits of resonance power supplies can cause the fault management software in two spacecraft to execute power-on resets in addition to other measures which can put the spacecraft in "safe mode" To address this issue without any design changes in the resonant power supplies, the culprit circuits need to be identified and correction of the fault management software needs to be implemented to account for the glitch effects. The goal is to "screen out" the effect of these glitches via software.

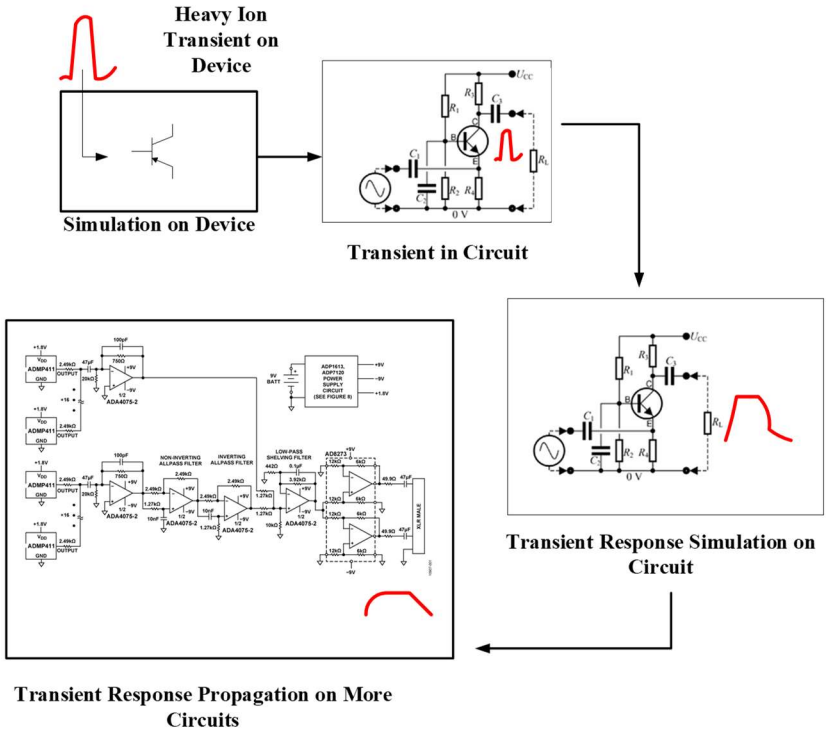

Figure 23. The effect of SET propagation from device level to whole assembly.

XIII SET HARDENING OF INTERCONNECTS

In PCB layout some of the standard techniques used to decrease crosstalk among circuits are wire sizing, spacing among circuits and wiring. Driver sizing should also be an effective technique for decreasing SET crosstalk noise and delay. For a fixed wire width, if a wire's spacing to its neighbors is increased, its coupling capacitance decreases while ground capacitance increases. Therefore, the reduction of spacing between wires and traces is an effective way in the reduction of SE crosstalk noise and delay, even though we pay some penalty due to use of routing resources. The wire sizing approach can also be used in mitigation of SET crosstalk. As a wire width is changed, its resistance and capacitances also changes. The larger wire size (i.e. width) causes a reduction in wire resistance and an increased in ground capacitance, all of which contribute to susceptible circuits' decreased susceptibility to noise. The wire-sizing approach, however, may not help the SET-induced crosstalk delay. This is because the increased ground capacitance of susceptible wire, will also cause an increase in delay if such capacitance is not also decreased.

Not all crosstalk mitigation approaches may be applicable to SET crosstalk noise and reduction. In crosstalk analysis, driver sizing can also be used to mitigate crosstalk effects. In case of an aggressor driver sizing method, if the driver is sized down, its effective trans conductance decreases. As a result, it cannot transition as fast due to its large resistance. Finally, the noise amount it induces on the victim line decreases.

XIV. MODELING SUBSYSTEM AND SYSTEM LEVEL EFFECTS FROM SET

The rigorous implementation of SET propagation effects as shown in Figure 23 is difficult to implement because it requires costly and time consuming SPICE-like simulations on multiple circuits with ever increasing complexities. Rather than providing a quantitative estimate of SET propagation across electronics of interest, a qualitative approach is pursued. In the qualitative approach the interest is mainly on the behavioral assessment of the circuits and the behavioral performance of such circuits. The SET effects are described in terms of behavioral responses which are first postulated at the circuit level and then extrapolated to higher level of complexities, such as the circuit card and then subsystem levels.

There are two methods to address subsystem and system levels effects from SET events in a behavioral approach. The first approach is the *Tabular model*. The Tabular model is quite good, and it has advantages with very little disadvantages. The main advantage of the Tabular model is that it emphasizes the outcome, including potential failures, without the need for transitional stages. The Tabular model is the most common approach used in the industry when performing SET analyses and a block diagram of the *Tabular model* is illustrated in Figure 24.

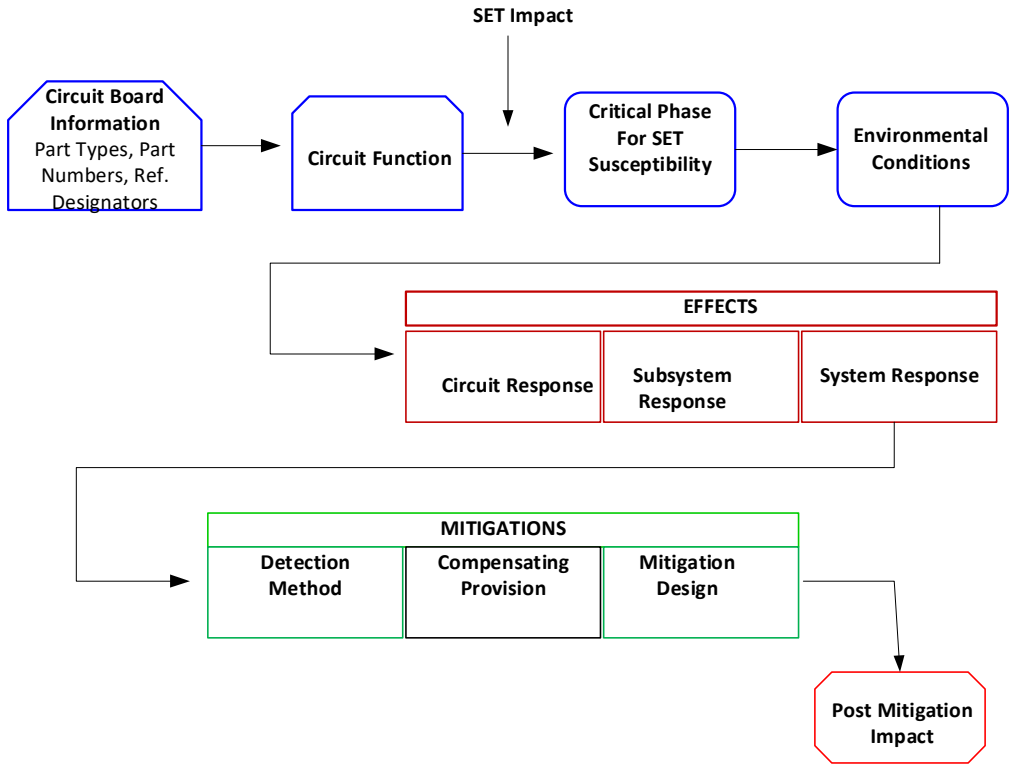

Figure 24. Flowchart on the use of the Tabular Model for assessing SET Effects.

An example of a tabular model addressing only the effects of a SET in a LM158A linear amplifier, which is part of a larger electronics assembly, is shown in Table 1.

Ref. No	SH	Sec.	Qty	Part Number	Part Function	SET Perturbation Assessed	SET Circuit Assessment	SET Subsystem Assessment	SET System Assessment
U2B	1	D4	2	LM158A	Main Loop Error Amp	≤±1V transient for 15 µsec on output	Transients of this magnitude and duration due to the inherent delays of the system, will have little effect on the output voltage. No effect at NHA.	No effect since transient will be filtered out	No effect
						Transients of greater magnitudes than +1V transient for 15 usec on output	Direct testing and analysis shows that for pulses on the input pin of the UC1864J shorter than 17.5µsec, the 5V main output will not trip, but may transition above the required point of regulation.	Regulation holds but at a higher voltage	No effect that can be observed if small

						Transients of magnitudes greater than -1V including transients to ground output	Due to the high gain of the feedback system at this point, a small negative transient at this point may cause a dip in the output voltage, possibly beyond acceptable regulation limits. Always voltages will remain within about 0.5V below nominal.	small period for out of regulation	drop output voltage by no more than 0.5V may affect low voltage circuits temporarily

Table 1. Example of Modeling SET propagation via a Tabular Model

The second approach is developed by this author; and it is identified as the SET *State Transition Model*. This author believes that the *State Transition Model* is much more revealing from a software engineering point of view and more rigorous when addressing SET propagation. The State Transition Model shows the states and the transitional probabilities to go from a fault-free state of the system to the actual failure state in multiple transitions. Figure 8 shows an example of the *State Transition Model*. The *State Transition Model* has the unique advantage that it can be mathematically, logically, and discretely represented via software models, and can be made into an intricate part of a fault management system.

The *Tabular Model* of Figure 24, which is the model used in the space industry, has the advantage that it allows for the analyst to propose mitigation effects to a SET event. The mitigation effect can be made in a qualitative manner. First, the analyst makes an assumption as to where in the hardware the SET event can be detected. Often that detection is not really observable (i.e. by flight software and/or fault protection software) until the SET event affects a subsystem or system functionality. The analyst then postulates a compensating provision that can be activated in software, hardware, or both in order to diminish, and if possible eliminate, the detrimental effect of the SET event. This compensating provision is most often achieved by a system level response (e.g. use of redundancy in the system). The analyst then explores the possibility, and can even suggest, if a design change is needed to address the effects of the SET, if the compensating provision is not adequate or the proposed design change is actually simple to implement. Once the SET effects have been mitigated either through a design change or an adequate compensating provision a post-mitigation impact is postulated at the mission level. As can be observed, the *Tabular Model* is hardware oriented and it is actually performed during the design stages of avionic hardware. The main goal in the *Tabular Model* is to identify potential hardware design changes that will diminish the effects of an SET.

The *State Transition Model* is a new model developed by this author and it is proposed for use in fault protection software development. The *State Transition Model* is software oriented. The main goal in the *State Transition Model* is to greatly improve the efficiency of fault protection software which is part of the flight software is a spacecraft. In the diagram of Figure 25 a SET which occurs inside the PWM of a dc/dc converter is tracked through a series of states nodes. The S0 node is not only the starting node but it is the node which identifies the PWM as working correctly. After a SET event, the *State Transition Model* shows the states S1 through S4, NOT as failure modes (as in the *Tabular model*), but rather as behavioral states of the PWM. These behavioral states can be monitored by a fault management software which can then diagnose,

very accurately, the SET propagation location; which is a capability that the *Tabular model* could not assess. The *State Transition* model also has another unique capability it allows for feedback among the transition states. These feedbacks are known as recovery modes (shown as recovery "R1- R6" modes in Figure 8). The recovery modes allow for SET annealing in case that at some point the hardware cleared the SET effect. Therefore, it allows for the fault management software to estimate the end location of the SET effect if annealing occurs.

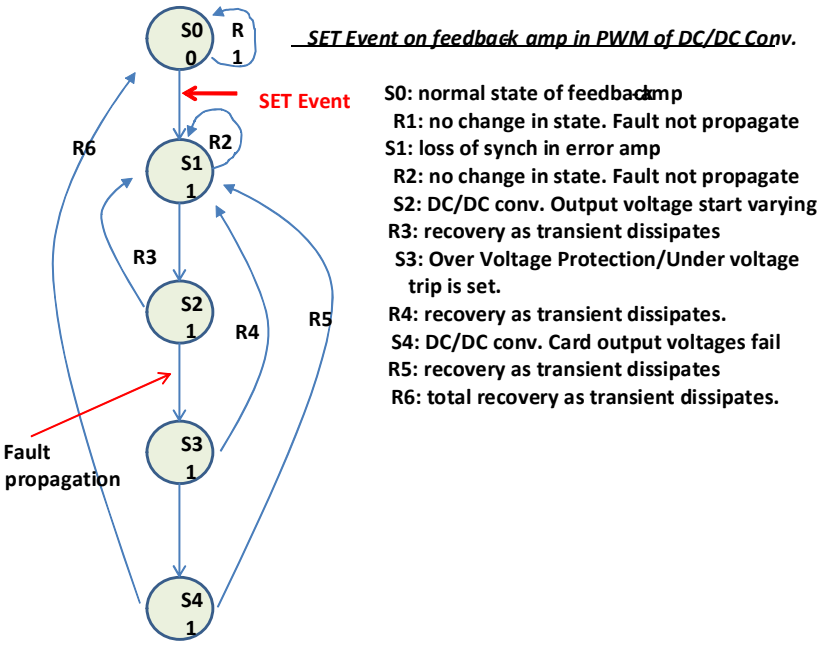

Figure 25. Example on the use of State Transition Diagram for modeling SET Effects.

XV ANALYSES AND PROTECTION FOR SET FOR ELECTRONIC DEVICES

Introduction

There are many methods to diminish the effects of SETs in the many different types of linear devices. The easiest and sometimes the most effective way to protect linear devices against SET is by filtering the output of the linear devices in order to eliminate the propagation of SET to other linear devices. For several applications, filtering may not be the correct approach and other techniques will need to be used. In some electronic devices, the susceptibility to SET and the transient behavior resulting from the SET are very much functions of the input and bias conditions of the electronic devices. A very simple way to decrease the transients in these electronic devices is to use input and biasing processes that are less susceptible to SETs. As with many other transient events, a powerful means to eliminate possible transients effects in digital electronics is to use a synchronous design. A few other mitigation methods in digital electronics that may be used for mitigating SET effects are triple majority voting, oversampling, and/or use software in an intelligent fashion. We now outline the effects of SET for different classes of electronic devices.

Voltage Comparators

It has been found in experimental research that the effect of a SET in a voltage comparator is a transient pulse at the output of the comparator that can have a worst case signature of a rail-to-rail change of state at the comparator output and the duration of the transient output is in the order of a few microseconds. In general, it has been noticed in experimental data that the lower the comparator differential input voltage, the greater is the device sensitivity to a SET event.

Operational Amplifiers

When an operational amplifier gets impacted by an SET its output experiences an output glitch. Experimental research over many years and extensive flight data from spacecraft missions has demonstrated that a great variety of transient outputs have been recorded (such as, positive-going transients, negative-going transients, or bipolar transients, with either short or long duration). The worst-case transient that has been observed has an amplitude to the power supply rail of the op-amp and with a duration of tens of microseconds normally. The SETs can be very difficult to mitigate in an analog circuits, specifically if the bandwidth of those circuits is wide compared to the SET transient pulse width. Therefore, the analysis of potential subsystem and system level effects and anomalies induced by a SET should be performed. If an operational amplifier is used in critical circuits a triple majority voting techniques and extensive filtering should be used where appropriate.

Voltage References

The effect of a SET in a voltage reference circuit is an output transient pulse. The best approach to mitigate such transient effects is by the addition of low pass filtering at the device output of the voltage reference circuit.

Voltage Regulators

The effect of a SET is an output transient pulse. SETs in voltage regulators, however, are generally filtered out by the large output capacitors used in most typical applications of voltage regulators. Therefore, there are no specific remediation used in most voltage regulators to eliminate or decrease the effects of SET.

MOSFET Drivers

There is no much experimental data available concerning SET for MOSFET drivers. MOSFET drivers are generally considered not to be very susceptible to SET. However, the use of MOSFET driver which could theoretically allow a destructive failure mode, like short circuit, due to a SET on the MOSFET driver should be avoided.

Analog-to-Digital/Digital-to-Analog Converters (ADC/DAC)

There are two possible mechanisms for SETs to propagate in ADCs. One of the most well known mechanisms for SEE in ADC/DAC is the SEU. The outcome at the output due to a SEU is most often observed as just a spread in the distribution of the digital output for a given analog input. In these cases a comparator in the converter is the most likely to have been hit and this causes the output to be shifted by a bit.

The other common mechanism that needs to be addressed is the case when the analog input is a rapidly varying input (in the time scale of a transient), and in this scenario a SET on the analog input of the ADC can be propagated through the entire chain of the ADC signaling and component. The SET manifests itself as the digital output of the ADC.

For DACs, the response to a SET is much simpler. Since on the output of the device we have an analog signal, the SET is manifested as the output transient of the analog output. It should be noted that these changes in the analog output of DACs are in addition to any SEU events that may be occurring. An upset can occur in the digital input latches of the DAC and that changes the state of the affected latch, causing a change in the analog output.

Line Drivers/Receivers/Transceivers

Line drivers and receivers are used for the transmission of data between two locations. Either at the source or at the end of the data transmission line, transients can be generated in the form of glitches in the data lines. At the end of transmission line SETs can place transients on the data line, that the receiver would have to see as valid data, for the error to propagate. A receiver can have an SET on its input side that glitch can then be interpreted as valid data. The primary mitigation for this class of parts is via software with data error detection and correction (EDAC).

Sample and Hold Devices

Sample and hold devices are designed to sample analog inputs and hold this information for use in ADC. The typical response of this type of device to SET would be having a transient form on the analog input of the device that the sample and hold circuitry that will use it cannot distinguish from the correct data. This means that any transient generated in the input would be locked into the output data. However, by their very nature, SETs are transient in nature, so over-sampling, redundant sampling, and majority voting can be used to counter these SET effects.

Timers

Timer devices are designed to produce pulsed output at specified time intervals. SETs can affect the output of timers by either placing glitches on the output pulse train or, even worst, by adding or removing pulses from the pulse train. Depending on the speed of the timer, glitches may or may not be a concern. However, the addition or the lack of pulses can affect system performance for those systems not designed to deal with these events.

Pulse Width Modulators (PWM)

There are three different types of SETs that have been identified in pulse width modulators (PWB): (1) both outputs go to a low output state condition for a period of time correlated with the soft start capability or the shutdown capability of the device. The time it takes for the duty cycle to increase from 0% to DC max after the SET event is equal to the time it takes to discharge and recharge the soft start capacitor in the soft start input circuit, (2) the second type of SET affecting PWM has a anomaly much shorter in duration. These short anomalies come in two forms. In the first type of anomaly, the both complementary outputs return to the low reference. This scenario lasts less than one clock period after which the PWM would return to normal output amplitude and frequency. The second form of upset manifests itself as a toggling of the outputs but not related to the clock. The correct function is restored before the next clock cycle begins, and (3) the third type of SET causes a phase shift of the clock circuit. The outputs follow the change in the clock phase. This scenario also affects the device frequency output. Therefore, depending on how the device is used in a circuit, this sort of SET upset can affect more than one function of the device.

For DC/DC converters which use PWM the two last types of SETs do not affect the operations of the DC/DC converters. This is due to the short duration of the event. However, the first type of SET could have an impact on the application depending on the soft start circuitry characteristics and design. The longer the duration of the soft start, the higher the impact on the application. It could be very critical on PWM devices where the user could not use the soft start circuitry. After shutdown, the device never starts again. The PWMs that do not implement the soft start and/or shutdown functions are not sensitive to these types of events. Figure 26 shows an example of a PWM in a dc/dc converter where SET could cause a detrimental behavior in the converter itself.

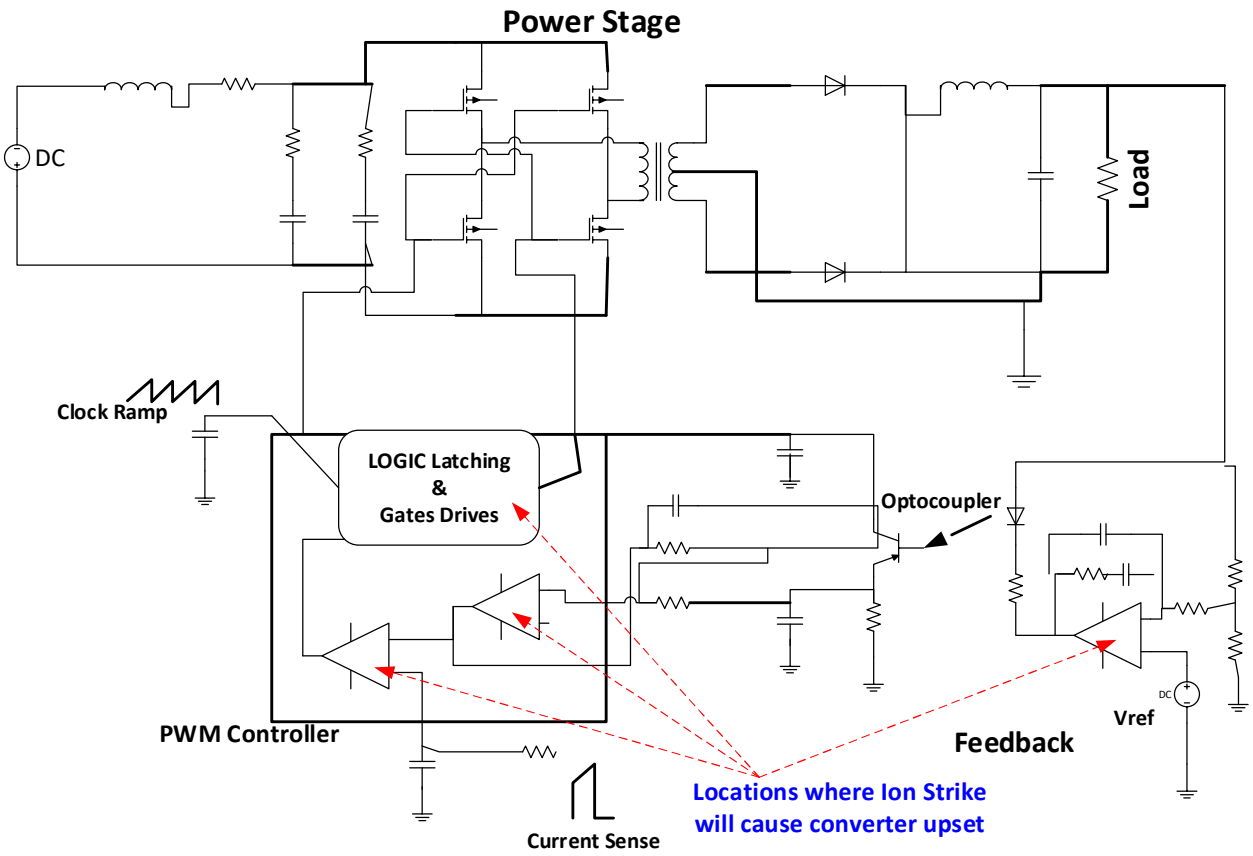

Figure 26. The effect of SET in PWM of a dc/dc converter.

Hybrid Devices

This classification of devices is generally assumed to be many types of devices. For example, there are linear devices that are of the hybrid design. Therefore, hybrid devices cover a large range of other types of devices, from simple devices such as optocoupler to more complex devices such as complex DC/DC converter, regulators, microcontrollers, etc. For each of these examples SETs are widely different.

Optocouplers can have their outputs susceptible to transients, which is typical of many types of linear devices, that transient varies widely with the application biasing. An oscillator can have either SETs as output glitches or extra or missing pulses, depending on which device within the oscillator has suffered the initial SET. DC/DC converters as previously stated can have simple transients on their outputs if the SET is generated in one of the devices near the output. Under some more severe case of SET susceptibility dc/dc converters can have output voltage dropouts, where the output voltage typically drops to zero. Though these dropouts can be short in durations (a few microseconds), it requires a reset of the converter to recover the normal output voltage.

Hybrid devices need to be selected very carefully for SET effects. A process needs to be established for the selection of linear devices that are either not susceptible or least susceptible to

SET. If a hybrid is selected that has unknown SET characteristics and utilized in an important system, radiation characterization for SETs will be required via radiation testing.

XVI. SEE TESTING OF SPACECRAFT HARDWARE ELECTRONICS

The IC's upset rates can cause actual damage to the component itself or to the system in a very strong radiation environment (e.g. solar flare). Therefore, prior testing of an IC for SEE is often done in electronic space systems design. This is a standard industry practice. IC testing is necessary because most commercially fabricated electronic components are not subjected to any kind of radiation survivability. SEE testing involves exposing the IC device to an ion beam from a particle accelerator as shown in Figure 27. Due to the short range of the charge ions, the IC must be de-lidded in order for the particles to reach the sensitive regions within the device. Tests are performed on de-lidded parts in a vacuum environment (simulating space). Several ions are used in testing and measuring the number of errors produced by the IC, and the total particle fluence is used to determine the cross-section at various LET values. A sample of the types of ions used in SEE testing is shown in Table 2. Single event testing is relatively straight forward for memory circuits. It is easy to define the internal conditions and to test the entire storage array of a memory circuit.

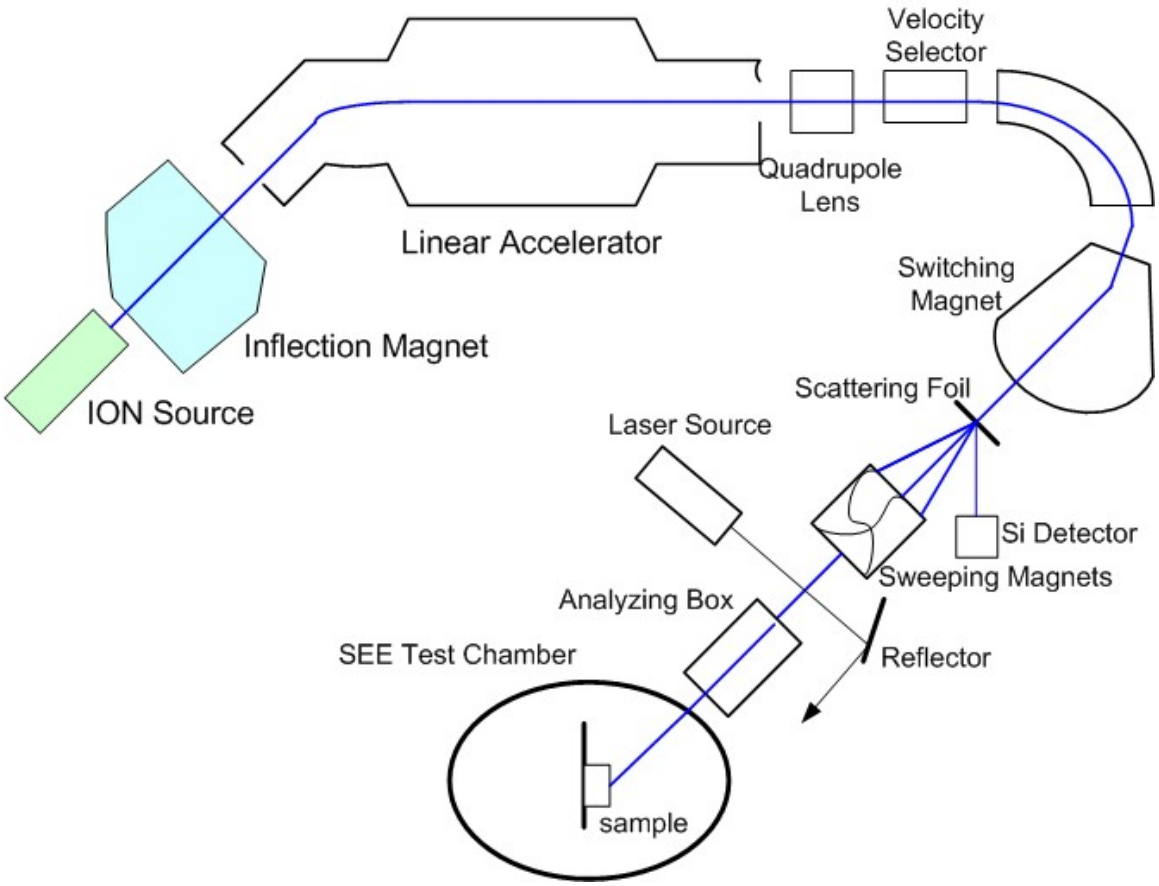

Figure 27. Layout of a high energy particle accelerator.

Very large scale integrated (VLSI) devices, such as microprocessors and random logic, are much more difficult to test. Bias conditions play a major role in single event upsets, particularly for

complex circuits. In order to interpret results, one must know which regions of a device involve internal storage cells and how many of them are being exercised during the test. For example, test results for some types of microprocessors have shown an order of magnitude increase in cross-section for a given LET when the device is exercised by operations that use cache memory compared to non-cache results. The LET can vary with incident angles and it is different for different devices.

Typical Ions used for SEE Testing				
Ion	**Atomic Number**	**Energy (MeV)**	**LET (MeV-cm^2/mg)**	**Range (um)**
Li	7	44	0.45	>100
C	12	105	1.39	202
F	19	150	3.02	133
Si	28	195	7.7	81
Cl	35	210	11.5	63
Ni	58	255	27	40.3
Br	79	285	37.3	36.4
Ag	107	300	53.1	30.9
I	127	230	59.9	30.7
Au	197	345	82.3	27.9

Table 2. Typical List of Ions used in SEE Testing by Particle Accelerators

The types of SEE that have been observed during testing in different types of ICs are shown in Table 3 [37].

Device Type	**Sensitive Area of Device**	**SEE Effects**
Memories	Memory cells	Bit flips
	Control logic	Bit flips if sequential, transients if combinatorial
Combinatorial Logic	Combinatorial logic	Transients
Sequential Logic	Sequential logic	Bit flips
FPGAs	Combinatorial logic	Transients
	Sequential logic	Bit flips
Microprocessors	Registers, cache, sequential control logic	Bit flips
ADC, DAC	Analog portion	Transients
	Digital portion	Bit flips or transients depending on design
Linear ICs	Analog area	Transients
Photodiodes	Photodiode	Transients
Optocouplers	Photodiode	Transients
Power MOSFETs	MOS	SEB, SEGR
FET Drivers	MOS	transients

Analog Switches	Analog portion	Momentarily switched state
Op-Amps, Comparators, and Voltage Regulators and References	Analog portion	Transients

Table 3. Sample Device Types, Sensitive Areas, and SEE

XVII CONCLUSION

This chapter addresses the physics of SET and its effects in digital electronics with a few examples. The chapter shows that SET events can be modeled in electronic circuits by first calculating the induced charge from a SET event and then using SPICE-like modeling tools to analyze the effects of such induced charge in the circuits themselves. The chapter discusses the modeling of an induced charge transient inside a digital gate and the modeling of an induced charge transient in a circuit. The chapter shows that transient propagation can affect multiple circuits in a chain, which is where the main problem relies in terms detrimental effects. The chapter also addresses the concept of crosstalk that could develop among digital circuits in the present of a SET event. The chapter also provides a brief discussion of SET hardening, a subject that needs much more coverage in the future. Finally, the paper focuses on SET propagation effects models and discusses two models, the Tabular and the State Transition Models. The State Transition model is a new methodology which uses state transition diagrams for tracking the effects of SET events through an electronics assembly and was developed in order to be easily incorporated with fault management software. Overall, the chapter shows that SETs are a potential risk for space missions now more than even because of the multiple ways its detrimental effects can be realized.

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